IN THE CLAIMS

Please amend the claims as follows:

1. (Canceled)

2. (Previously Presented) A clock phase interpolator circuit comprising:

a first plurality of differential transistor pairs, a first plurality of select transistors, and a first current source, the first current source coupled to each of the first plurality of differential transistor pairs through one of the first plurality of select transistors; and

a second plurality of differential transistor pairs, a second plurality of select transistors, and a second current source, the second current source coupled to each of the second plurality of differential transistor pairs through one of the second plurality of select transistors, wherein each differential transistor pair is configured to receive a different phase of a clock signal.

3. (Original) The clock phase interpolator circuit of claim 2 further comprising a control circuit to select one of the first plurality of differential transistor pairs and one of the second plurality of differential transistor pairs.

4. (Original) The clock phase interpolator circuit of claim 3 wherein the first and second current sources are variable current sources.

5. (Original) The clock phase interpolator circuit of claim 4 wherein the control circuit includes output nodes coupled to the first and second current sources to control currents sourced thereby.

6. (Original) The clock phase interpolator circuit of claim 4 wherein the first current source comprises a plurality of parallel-coupled current source transistors, each being individually selectable.

7. (Original) The clock phase interpolator circuit of claim 2 further comprising a differential amplifier coupled to output nodes of both the first and second plurality of differential transistor pairs.

8. (Original) The clock phase interpolator circuit of claim 7 wherein the first and second current sources are constant current sources.

9. (Currently Amended) A clock recovery circuit comprising:

an input clock node to receive a clock signal and an output clock node;

a first circuit to generate multiple clock phases from the clock signal on the input clock node;

a phase detector and control circuit to compare a phase of a data signal and a phase of a clock signal on the output clock node, and to create interpolator control signals, the phase detector including a clock node to receive the clock signal from the ~~input~~ output clock node, and a data node to receive the data signal; and

an interpolator circuit with a plurality of differential transistor pairs operative to switch current responsive to the multiple clock phases and interpolator control signals, to drive an output clock on the output clock node, wherein at least one first differential transistor pair of the plurality of differential transistor pairs is responsive to a first clock phase of the multiple clock phases, and wherein at least one second differential transistor pair of the plurality of differential transistor pairs is responsive to a second clock phase of the multiple clock phases.

10. (Currently Amended) A clock recovery circuit comprising:

an input clock node to receive a clock signal and an output clock node;

a first circuit to generate multiple clock phases from the clock signal on the input clock node;

a phase detector and control circuit to compare a phase of a data signal and a phase of a clock signal on the output clock node, and to create interpolator control signals, the phase

detector including a clock node to receive the clock signal from the output clock node, and a data node to receive the data signal; and

an interpolator circuit with a plurality of differential transistor pairs operative to switch current responsive to the multiple clock phases and interpolator control signals, to drive an output clock on the output clock node, ~~The clock recovery circuit of claim 9~~ wherein the interpolator circuit comprises [[:]] a first differential transistor pair responsive to a first clock phase, and a second differential transistor pair responsive to a second clock phase.

11. (Original) The clock recovery circuit of claim 10 wherein the interpolator circuit further comprises:

a first current source coupled to the first differential transistor pair; and

a second current source coupled to the second differential transistor pair.

12. (Original) The clock recovery circuit of claim 11 wherein the first and second current sources are variable current sources responsive to the interpolator control signals.

13. (Previously Presented) The clock recovery circuit of claim 11 wherein the first and second current sources are constant current sources.

14. (Previously Presented) A clock recovery circuit comprising:

an input clock node and an output clock node;

a first circuit to generate multiple clock phases from a clock signal on the input clock node;

a phase detector and control circuit to compare a phase of a data signal and a phase of a clock signal on the output clock node, and to create interpolator control signals; and

an interpolator circuit with a plurality of differential transistor pairs operative to switch current responsive to the multiple clock phases and interpolator control signals, to drive an output clock on the output clock node, wherein the interpolator circuit further comprises:

a first plurality of differential transistor pairs having differential output nodes coupled in common;

a first current source coupled to source current through the first plurality of differential transistor pairs;

a second plurality of differential transistor pairs having differential output nodes coupled in common with the differential output nodes of the first plurality of differential transistor pairs;

a second current source coupled to source current through the second plurality of differential transistor pairs; and

a differential amplifier coupled to the differential output nodes to drive the output clock on the output clock node.

15. (Original) The clock recovery circuit of claim 14 further comprising a separate select transistor coupled between each differential transistor pair and a respective current source, the select transistors being responsive to the interpolator control signals.

16. (Previously Presented) The clock recovery circuit of claim 14 wherein the first and second current sources are fixed current sources.

17. (Previously Presented) The clock recovery circuit of claim 14 wherein the first and second current sources are variable current sources having input nodes responsive to the interpolator control signals.

18. (Canceled)

19. (Previously Presented) An integrated circuit comprising:

a first differential transistor pair to receive a first clock signal at a first phase, the first differential transistor pair having a first differential output node;

a second differential transistor pair to receive a second clock signal at a second phase, the second differential transistor pair having a second differential output node coupled in common with the first differential output node;

a first variable current source coupled to the first differential transistor pair;

a second variable current source coupled to the second differential transistor pair;

a differential amplifier having a differential input node coupled to the first differential output node; and

a third differential transistor pair coupled in parallel with the first differential transistor pair between the first differential output node and the first current source.

20. (Original) The integrated circuit of claim 19 further comprising:

a fourth differential transistor pair coupled in parallel with the second differential transistor pair between the second differential output node and the second current source.

21. (Original) The integrated circuit of claim 20 further comprising:

a first select transistor coupled between the first differential transistor pair and the first current source;

a second select transistor coupled between the second differential transistor pair and the second current source;

a third select transistor coupled between the third differential transistor pair and the first current source; and

a fourth select transistor coupled between the fourth differential transistor pair and the second current source.

22. (Original) The integrated circuit of claim 21 further comprising a control circuit to select one of the first and second select transistors, and one of the third and fourth select transistors, and to select a first current to be provided by the first current source, and to select a second current to be provided by the second current source.

23. (Previously Presented) The integrated circuit of claim 19 further comprising a delay locked loop circuit coupled to the first and second differential transistor pairs, to provide the first and second clock signals from a received clock signal.

24. (Original) The integrated circuit of claim 23 further comprising a phase detector having input nodes coupled to an output node of the differential amplifier and to a data node to receive a data signal, and having an output node to provide a phase error signal.

25. (Original) The integrated circuit of claim 24 further comprising a control circuit to receive the phase error signal and to control the first and second variable current sources.

26. (Original) The integrated circuit of claim 25 wherein the phase comparator provides a digital error signal.

27. (Original) The integrated circuit of claim 25 wherein the phase comparator provides an analog error signal.

28. (Original) The integrated circuit of claim 27 wherein the control circuit includes an analog-to-digital converter.